Listing of the Claims:

1. (Previously Presented) A method of forming a cell pad contact hole on an integrated circuit, comprising:

forming adjacent gates on an integrated circuit substrate having a source/drain region extending between the gates;

forming gate spacers on facing sidewalls of the adjacent gates;

forming a cell pad contact hole aligned to the gates and gate spacers that exposes the source/drain region in the integrated circuit substrate;

forming a first poly film in the cell pad contact hole;

forming a region in the source/drain region by ion-implanting through the first poly film; and

forming a second poly film on the first poly film that substantially fills the cell pad contact hole.

2. (Original) The method of Claim 1 wherein the gate spacers are formed from a nitride film.

3. (Original) The method of Claim 1 wherein the source/drain region comprises an N-type source/drain region overlapping the gates.

4. (Original) The method of Claim 1 further comprising forming an insulating film that planarizes undulations from the gates before forming a cell pad contact hole.

5. (Original) The method of Claim 4 further comprising etching the first and second poly films to expose an upper surface of the insulating film.

6. (Original) The method of Claim 4 wherein forming the first poly film comprises conformably forming the first poly film in the cell pad contact hole.

7. (Original) The method of Claim 4 wherein the first poly film comprises an undoped poly film.

8. (Original) The method of Claim 4 wherein the first poly film comprises a doped poly film.

9. (Original) The method of Claim 8 wherein a concentration of dopants in the first poly film is lower than a concentration of dopants in the second poly film.

10 (Previously Presented) The method of Claim 4 wherein forming the first poly film comprises forming the first poly film to a thickness selected to provide a desired depth of the region formed by ion implanting.

11. (Original) The method of Claim 4 wherein forming the adjacent gates comprises:

forming a poly film of the gates on the integrated circuit substrate;

forming a tungsten silicide (WSi) film of the gates on the poly film of the gates; and

forming a nitride film of the gates on the tungsten silicide film.

12. (Original) The method of Claim 4 further comprising:

forming an additional insulating layer on the first poly film, the second poly film and the insulating layer;

forming a buried contact hole in the additional insulating layer that exposes an upper surface of the second poly film;

forming a contact poly film in the buried contact hole; and

etching the contact poly film to expose an upper surface of the additional insulating layer.

13-26. (Canceled)

27. (Previously Presented) A fabrication method of a semiconductor device having a cell pad contact hole, the method comprising:

preparing a semiconductor substrate having an device isolating film, a pair of gates adjacent each other, gate spacers on the gates, and an insulating film on the gates and gate spacers, wherein N-type source/ drains are formed in the semiconductor substrate between the gates;

forming a cell pad contact hole self-aligned to the gates and the gate spacers in the insulating film so that the semiconductor substrate is exposed;

conformably forming a first poly film in the cell pad contact hole;

forming a region through an ion implanting process performed on the first poly film;

forming a second poly film on the second poly film; and

etching back on the first and the second poly films to expose an upper surface of the insulating film, so that the cell pad contact hole is filled with the first and the second poly films.

28. (Previously Presented) The method of Claim 27, wherein the first poly film is an undoped poly film.

29. (Previously Presented) The method of Claim 27, wherein the first poly film is a doped poly film.

30. (Previously Presented)The method of Claim 27, wherein a concentration of the first poly film is lower than that of the second poly film.

31. (Previously Presented) The method of Claim 27, wherein a depth of the region formed through an ion implanting is controlled by thickness of the first poly film.

32. (Previously Presented) A method of forming a cell pad contact hole on an integrated circuit, comprising:

forming adjacent gates on an integrated circuit substrate and forming a source/drain region extending between the gates;

forming gate spacers on facing sidewalls of the adjacent gates;

forming a cell pad contact hole aligned to the gates and gate spacers that exposes the source/drain region in the integrated circuit substrate;

forming a first poly film in the cell pad contact hole;

forming a region in the source/drain region by ion-implanting through the first poly film; and

forming a second poly film on the first poly film that substantially fills the cell pad contact hole.

33. (Previously Presented) The method of Claim 32 wherein the gate spacers are formed from a nitride film.

34. (Previously Presented) The method of Claim 32 wherein the source/drain region comprises an N-type source/drain region overlapping the gates.

35. (Previously Presented) The method of Claim 32 further comprising forming an insulating film that planarizes undulations from the gates before forming a cell pad contact hole.

36. (Previously Presented) The method of Claim 35 further comprising etching the first and second poly films to expose an upper surface of the insulating film.

37. (Previously Presented) The method of Claim 35 wherein forming the first poly film comprises conformably forming the first poly film in the cell pad contact hole.

38. (Previously Presented) The method of Claim 35 wherein the first poly film comprises an undoped poly film.

39. (Previously Presented) The method of Claim 35 wherein the first poly film comprises a doped poly film.

40. (Previously Presented) The method of Claim 39 wherein a concentration of dopants in the first poly film is lower than a concentration of dopants in the second poly film.

41 (Previously Presented) The method of Claim 35 wherein forming the first poly film comprises forming the first poly film to a thickness selected to provide a desired depth of the region formed by ion implanting.

42. (Previously Presented) The method of Claim 35 wherein forming the adjacent gates comprises:

forming a poly film of the gates on the integrated circuit substrate;

forming a tungsten silicide (WSi) film of the gates on the poly film of the gates; and

forming a nitride film of the gates on the tungsten silicide film.

43. (Previously Presented) The method of Claim 35 further comprising:

forming an additional insulating layer on the first poly film, the second poly film and the insulating layer;

forming a buried contact hole in the additional insulating layer that exposes an upper surface of the second poly film;

forming a contact poly film in the buried contact hole; and

etching the contact poly film to expose an upper surface of the additional insulating layer.